JTN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,111	03/06/2002	Stewart R. Wyatt	10018461-1	8005

7590 03/30/2005

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
MCCARTHY, CHRISTOPHER S	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,111	WYATT ET AL.	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-16 and 19-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-16,19-26,28-38 and 40-42* is/are rejected.

7)☒ Claim(s) *27,39 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 11-16, 19-26, 28-38, and 40-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Fanning U.S. Patent 6,816,986.

2. Claims 27, 39, and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Objections

3. Claim 14 is objected to because of the following informalities: problematic language is found in the preamble as it reads "the comprising which are executable". Appropriate correction is required.

4. Claim 15 is objected to because of the following informalities: the claim language is problematic as it reads "verifying comprises repeatedly verifying comprises until an error is detected". Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 11-16, 19-26, 28-38, and 40-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Fanning U.S. Patent 6,816,986.

As per claim 11, Fanning teaches a system for verifying data in a data storage device, the data storage device storing data in a number of accessible address locations, said system comprising: means for designating a range of addresses from said number of accessible address locations as addresses to be verified (column 5, line 63 – column 6, line 34); means for verifying whether or not data stored in a starting address of said addresses to be verified contains an error (column 6, lines 31-34); means for incrementing the verified address (column 5, line 65 – column 6, line 3); means for determining whether or not the incremented address is at the end of the range of addresses to be verified (column 6, lines 21-26); means for changing the address to the next address when said means for determining has determined that the incremented address is not at the end of the range of addresses to be verified (column 5, line 65 – column 6, line 3); and means for resetting the address to an address at the start of the range of addresses to be verified when said means for determining has determined that the address is at the end of the range of addresses to be verified such that all addresses within the range can be re-verified in a continuous loop (column 6, lines 27-29, wherein, the predetermined number could include indefinite range, such as infinity).

As per claim 12, Fanning teaches the system of claim 11, further comprising means for counting the number of errors detected by said means for verifying (column 6, lines 30-34).

As per claim 13, Fanning teaches the system of claim 11, further comprising means for storing output results from said means for verifying (column 6, lines 30-34).

As per claim 14, Fanning teaches a computer-readable medium containing computer-readable instructions [the comprising] which are executable to: input a starting address and an ending address so as to define a range of addresses to be verified (column 6, lines 21-26); verify whether or not data stored at an address in the range contains an error (column 6, lines 31-34); determine whether or not the verified address is the ending address (column 6, lines 21-28); and initiate verification of the first address if the verified address is the ending address such that all addresses within the range can be re-verified in a continuous loop (column 6, lines 27-29).

As per claim 15, Fanning teaches the computer-readable medium of claim 14, wherein verifying comprises repeatedly verifying [comprises] until an error is detected (column 6, lines 30-34).

As per claim 16, Fanning teaches the computer-readable medium of claim 14, further comprising instructions executable to initiate an interrupt upon detection of an error by said logic configured to verify, wherein initiating an interrupt comprises correcting the data detected in the error (column 5, lines 11-19, wherein, the correction process is the replace the faulty device).

As per claim 19, Fanning teaches a computer-implemented method for verifying data stored in a data storage device, comprising: sequentially verifying whether or not data stored at multiple addresses within a range of addresses defined by a starting address and an ending address contains an error; and continuously repeating the sequential verifying of the multiple

addresses within the range in a continuous loop such that the verifying can continue indefinitely (column 5, line 63 – column 6, line 34).

As per claim 20, Fanning teaches the method of claim 19, wherein verifying comprises verifying the addresses using an error code correction (ECC) encoder/decoder (column 6, lines 40-42).

As per claim 21, Fanning teaches the method of claim 19, wherein verifying the addresses using an error code correction (ECC) encoder/decoder comprises writing encoded data that is stored at the addresses, reading the stored encoded data from the addresses, decoding the encoded data, and identifying any errors in the data (column 6, lines 21-42).

As per claim 22, Fanning teaches the method of claim 21, further comprising correcting any errors in the data (column 5, lines 11-19).

As per claim 23, Fanning teaches the method of claim 19, wherein the range of addresses comprises a subset of all of the addresses of the data storage device (column 6, lines 21-25; column 4, lines 8-14).

As per claim 24, Fanning teaches the method of claim 19, wherein the range of addresses comprises all of the addresses of the data storage device (column 6, lines 21-25).

As per claim 25, Fanning teaches the method of claim 19, further comprising collecting data regarding errors in data stored at one or more of the multiple addresses without interrupting the sequential verifying (column 6, lines 31-34).

As per claim 26, Fanning teaches the method of claim 19, further comprising interrupting the sequential verifying upon detecting an error in data of one of the multiple addresses (column 5, lines 11-19).

As per claim 28, Fanning teaches the method of claim 19, further comprising terminating the sequential verifying upon an external error occurring (column 5, lines 11-19).

As per claim 29, Fanning teaches the method of claim 19, further comprising terminating the sequential verifying upon completion of verifying each address in the range a predetermined number of times (column 6, lines 27-29).

As per claim 30, Fanning teaches the method of claim 19, further comprising receiving designation of the start address and the end address (column 6, lines 21-25).

As per claim 31, Fanning teaches a memory component, comprising: a data storage device that includes a plurality of addresses; and a storage device controller that includes an error correction code (ECC) encoder/decoder and a verify module, the verify module comprising a processor that controls the ECC encoder/decoder to sequentially verify whether or not data stored at addresses of the data storage devices within a range defined by a starting address and an ending address contains an error, and to continuously repeat the sequential verifying of the multiple addresses within the range in a continuous loop such that the verifying can continue indefinitely (column 5, line 63 – column 6, line 44).

As per claim 32, Fanning teaches the memory component of claim 31, wherein the data storage device is a solid state storage device (column 3, lines 28-37).

As per claim 33, Fanning teaches the memory component of claim 31, wherein the data storage device is a magnetic storage device (column 2, line 65 – column 3, line 3).

As per claim 34, Fanning teaches the memory component of claim wherein the ECC encoder/decoder is configured to write encoded data that is stored at the addresses, read the

stored encoded data from the addresses, decode the encoded data, and identify any errors in the data (column 6, lines 21-42).

As per claim 35, Fanning teaches the memory component of claim 34, wherein the ECC encoder/decoder is further configured to correct any errors in the data (column 5, lines 11-19).

As per claim 36, Fanning teaches the memory component of claim 31, wherein the verify module further comprises an address counter that stores the starting address (column 4, lines 51-53; column 6, lines 21-25).

As per claim 37, Fanning teaches the memory component of claim 31, wherein the verify module further comprises at least one counter that stores at least one pf an indication of the number of times each address within the range is to be verified and the number of data errors that are detected (column 6, lines 31-34).

As per claim 38, Fanning teaches the memory component of claim 31, wherein the verify module further comprises a configuration register that stores data used to configure the ECC encoder/decoder (column 6, lines 31-34).

As per claim 40, Fanning teaches the memory component of claim 31, wherein the range of addresses comprises a subset of all of the addresses of the data storage device (column 6, lines 21-25; column 4, lines 8-14).

As per claim 41, Fanning teaches the memory component of claim 31, wherein the range of addresses comprises all of the addresses of the data storage device (column 6, lines 21-25).

As per claim 42, Fanning teaches the memory component of claim wherein the ECC encoder/decoder is further configured to interrupt the sequential verify upon detecting an error in data of one of the addresses (column 6, lines 41-48).

Allowable Subject Matter

7. Claims 27, 39, and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims 11-16, 19-43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: See attached PTO-892.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
March 28, 2005

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100